METHOD AND STRUCTURE FOR IMPROVING LATCH-UP IMMUNITY USING NON-DOPANT IMPLANTS

ABSTRACT

The preferred embodiment of the present invention overcomes the limitations of the prior art and provides a device and method to increase the latch-up immunity of CMOS devices by forming a non-dopant region near the edge of a dopant region. The preferred embodiment method to increase the latch-up immunity of CMOS devices uses hybrid photoresist to selectively form non-dopant implants near the edges of the N-well and/or P-well. The non-dopant implants suppress diffusion of dopant in the wells resulting in greater control of well spacing, and hence reducing the gain of the parasitic transistor. This reduces the propensity of the CMOS device to latch-up. The preferred embodiment method allows the non-dopant implants to be formed without requiring additional masking steps over the prior art methods.